IN THE CLAIMS

1. (Currently Amended) An encryption circuit, comprising:

a plurality of operation circuits which are connected; and

a control circuit dividing data to plural parts for providing to each of said plurality of operation circuits and controlling said plurality of operation circuits to provide encryption or decryption control; wherein

each of said plurality of operation circuits includes

a first register holding corresponding part of data as operation data,

an addition and subtraction circuit performing addition and subtraction with respect to the operation data held in said first register,

a right-shift circuit performing right-shift with respect to an operation result by said addition and subtraction circuit, and

a second register holding an operation result by said right-shift circuit,[[;]]

~~an~~ wherein said addition and subtraction circuit in a first operation circuit performs addition and subtraction using a carry-in signal supplied from a second operation circuit, and outputs a carry-out signal as said carry-in signal of ~~generated through addition and subtraction to~~ a third operation circuit; and

a right-shift circuit in said first operation circuit performs right-shift using a right shift-in signal supplied from ~~a right shift circuit in~~ said third operation circuit, and outputs a right shift-out signal as said right shift-in signal of ~~generated through right shift to a right shift circuit in~~ said second operation circuit.

Claim 2 (cancelled)

3. (Currently Amended) The encryption circuit according to claim 1, wherein

said addition and subtraction circuit in said first operation circuit determines the operation data at a first clock, and

~~an~~ said addition and subtraction circuit in said third operation circuit determines the operation data with said carry-in signal supplied ~~and a carry-out~~ from said first operation circuit at a second clock delayed by one dock from said first clock.

4. (Original) The encryption circuit according to claim 1, wherein

said addition and subtraction circuit in said first operation circuit determines the operation data at the first clock, and

in the second register in said first operation circuit, a bit except for a most significant bit is written at the second clock delayed by one clock from said first clock, and the most significant bit is written at a third clock delayed by half clock from said second clock.

5. (Currently Amended) The encryption circuit according to claim 1, wherein

said plurality of operation circuits are connected such that said carry-in signal and said shift-in signal ~~a carryout signal and a shift-out signal~~ form a loop.

6. (Currently Amended) The encryption circuit according to claim 1, wherein

respective one of said plurality of operation circuits further includes a left-shift circuit performing left-shift with respect to the operation result held in said second register, and

~~a~~ said left-shift circuit in said first operation circuit performs left-shift using a left shift-in signal supplied from said second operation circuit, and outputs a left shift-out signal as said left shift-in signal of ~~generated through left-shift to~~ said third operation circuit.

7. (Currently Amended) The encryption circuit according to claim 6, wherein

said first operation circuit further includes a selector selectively outputting one of said left ~~a~~ shift-in signal from said second ~~third~~ operation circuit and said left shift-out ~~a shift-in~~ signal from the left-shift circuit in said first operation circuit to the addition and subtraction circuit in said first operation circuit.